

FILE 'REGISTRY' ENTERED AT 13:48:59 ON 17 FEB 2004

L1 8 S AL2O3/MF
 L2 127 S AL.O/MF
 L3 3 S O3Y2/MF
 L4 65 S O.Y/MF
 L5 27 S O.SI.ZR/MF
 L8 8 S HF.O.SI/MF
 L10 4 S LA2O3/MF
 L11 21 S LA.O/MF
 L12 14 S O2ZR/MF
 L13 109 S O.ZR/MF
 L14 7 S HFO2/MF
 L15 25 S HF.O/MF
 L16 3 S O5TA2/MF
 L17 106 S O.TA/MF
 L18 1 S O3PR2/MF
 L19 53 S O.PR/MF
 L20 17 S O2TI/MF
 L21 280 S O.TI/MF
 L23 48 S O2SI/MF
 L25 345 S O.SI/MF
 L26 3227 S AL O/ELF
 L27 1737 S O Y/ELF
 L28 102 S O SI ZR/ELF
 L30 28 S HF O SI/ELF
 L31 282 S LA O/ELF
 L32 1058 S O ZR/ELF
 L33 163 S HF O/ELF
 L34 315 S O TA/ELF
 L35 88 S O PR/ELF
 L36 991 S O TI/ELF
 L37 19866 S O SI/ELF

FILE 'DPCI' ENTERED AT 13:50:06 ON 17 FEB 2004

L38 1 S US 6008091/PN
 L39 SEL L38 1- PN : 5 TERMS
 L40 1 S L39
 L41 SEL L38 1- PN.G : 8 TERMS
 L42 SEL L38 1- PN.D : 9 TERMS
 L43 8 S L41/PN
 L44 9 S L42/PN
 L45 17 S (L43 OR L44)
 L46 SEL L45 1- PN.G : 599 TERMS
 L47 473 S L46/PN
 L48 SEL L47 1- PRN : 713 TERMS

FILE 'HCAPLUS, WPIX' ENTERED AT 14:28:32 ON 17 FEB 2004

L49 847 S L48
 L50 157271 S (DIELEC? OR KAPPA OR K OR PERMIT#####) (6A)
 (STACK? OR SANDWICH? OR LAYER? OR MULTILAYER? OR FILM? OR
 LAMINA#####)
 L51 225 S L49 AND L50
 L52 165777 S (FORBIDDEN OR ENERG#####) (2A) (GAP# OR
 BAND#) OR BANDGAP# OR EG OR LATTICE#(2A) CONSTANT#
 L53 0 S L51 AND L52
 L54 9 S L49 AND L52

FILE 'REGISTRY' ENTERED AT 14:40:44 ON 17 FEB 2004

L55 27288 S (L1 OR L2 OR L3 OR L4 OR L5 OR L6 OR L7 OR
L8 OR L9 OR L10 OR L11 OR L12 OR L13 OR L14 OR L15 OR L16 OR
L17 OR L18 OR L19 OR L20 OR L21 OR L22 OR L23 OR L24 OR L25 OR
L26 OR L27 OR L28 OR L29 OR L30 OR L31 OR L32 OR L33 OR L34 OR
L35 OR L36 OR L37)

L56 SEL L55 1- RN : 27288 TERMS

FILE 'HCAPLUS, WPIX' ENTERED AT 15:00:15 ON 17 FEB 2004

L58 778230 S L56

L59 2 S L58 AND L54

L60 63 S L51 AND L58

L61 153589 S DIELECT?(2A) CONSTANT? OR (HIGH OR LOW) (2A) (K OR PERMITT##### OR
KAPPA)

L62 13 S L60 AND L61

L63 15 S L59 OR L62

L64 15 DUP REMOVE L63 (0 DUPLICATES REMOVED)

SYSTEM:OS - DIALOG OneSearch

File 2:INSPEC 1969-2004/Feb W1
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File 6:NTIS 1964-2004/Feb W2
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File 8:Ei Compendex(R) 1970-2004/Feb W1
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File 25:Weldasearch 1966-2002/Aug
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File 34:SciSearch(R) Cited Ref Sci 1990-2004/Feb W2
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File 434:SciSearch(R) Cited Ref Sci 1974-1989/Dec
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File 35:Dissertation Abs Online 1861-2004/Jan
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File 103:Energy SciTec 1974-2004/Feb B1
(c) 2004 Contains copyrighted material

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(c) 2004 INIST/CNRS

File 239:Mathsci 1940-2004/Mar
(c) 2004 American Mathematical Society

File 241:Elec. Power DB 1972-1999Jan
(c) 1999 Electric Power Research Inst.Inc

File 305:Analytical Abstracts 1980-2004/Jan W1
(c) 2004 Royal Soc Chemistry

File 315:ChemEng & Biotec Abs 1970-2004/Jan
(c) 2004 DECHEMA

File 354:Ei EnCompassLit(TM) 1965-2004/Feb W1
(c) 2004 Elsevier Eng. Info. Inc.

File 987:TULSA (Petroleum Abs) 1965-2004/Feb W3
(c)2004 The University of Tulsa

Set	Items	Description
S1	9420	CONTROL????(2N)GATE? ?
S2	1637	DIELECTRIC(2N)STACK?
S3	4727	FLOAT????(2N)GATE? ?
S4	547	TUNNEL????(2N)OXIDE? ?(2N)LAYER? ?
S5	1208273	SUBSTRAT???
S6	280001	(FORBIDDEN OR ENERG????)(2N)(GAP? ? OR BAND? ?) OR BANDGAP? ? OR EG OR LATTICE? ?(2N)CONSTANT? ?
S7	364392	DIELECTRIC(2N)CONSTANT? OR (HIGH OR LOW)(2N)K OR PERMITT??- ?????
S8	6524	(SECOND? OR ADDITIONAL? OR FURTHER?)(2N)OXIDE? ?
S9	0	S1 AND S2 AND S3 AND S4 AND S5 AND S6 AND S7
S10	0	S1 AND S2 AND S3 AND S5 AND S6 AND S7
S11	1	S1 AND S3 AND S5 AND S6 AND S7
S12	1	S1 AND S3 AND S6 AND S7
S13	1	S11 OR S12
S14	12	S1 AND S3 AND S6:S7
S15	11	S14 NOT S13
S16	6	RD (unique items)
S17	19020	(NONVOLATILE OR FLASH)(2N)MEMOR??? OR EPROM OR EEPROM
S18	7	S17 AND S6 AND S7
S19	7	S18 NOT S14
S20	6	RD (unique items)
S21	858487	MEMOR??? OR PROM OR PROMS OR ROMS OR ROM OR RAM OR SRAM OR DRAM OR EPROM OR EPROMS OR EEPROM OR EEPROMS OR STOR??? (2N) (I- NFORMATION OR DATA)
S22	71	S21 AND S6 AND S7 NOT S18
S23	54	RD (unique items)
S24	45	S23 NOT PY>2001

Set	Items	Description
S1	1388619	SWITCH? OR FLIPFLOP? OR FLIP() FLOP? OR TOGGLE? OR BRIDGE? - OR GATE?
S2	245408	STACK?
S3	2343626	LAYER?
S4	3232	(E OR EE) () PROM? ? OR BUBBLE() (STORAGE OR MEMOR?)
S5	109056	BAND() GAP?
S6	0	S1 AND S2 AND S3 AND S4 AND (S5 OR PERMITT? OR DIELECTRIC - OR DIE() ELECTRIC)
S7	978	S1 AND S2 AND S3 AND (S5 OR PERMITT? OR DIELECTRIC OR DIE(-) ELECTRIC OR BANDGAP?)
S8	0	S4 AND S7

S1	314041	GATE? ?
S2	245409	STACK?
S3	280001	(FORBIDDEN OR ENERG????) (2N) (GAP? ? OR BAND? ?) OR BANDGAP? ? OR EG OR LATTICE? ? (2N) CONSTANT? ?
S4	364392	DIELECTRIC (2N) CONSTANT? OR (HIGH OR LOW) (2N) K OR PERMITT??- ?????
S5	969164	NON(W) VOLATILE OR NONVOLATILE OR FLASH OR MEMOR??? OR PROM OR PROMS OR ROMS OR ROM OR RAM OR SRAM OR DRAM OR EPROM OR EP- ROMS OR EEPROM OR EEPROMS OR STOR??? (2N) (INFORMATION OR DATA) OR BUBBLE(W) STORAGE
S6	1	S1 AND S2 AND S3 AND S4 AND S5

115930

ETC

SEARCH REQUEST FORM Scientific and Technical Information Center - EIC2800

Rev. 8/27/01 This is an experimental format -- Please give suggestions or comments to Jeff Harrison, CP4-9C18, 306-5429.

Date 2/2/04 Serial # 091990,397 Priority Application Date 20010504
 Your Name M. Lewis Examiner # _____
 AU 2829 Phone 202-1838 Room 5A30
 In what format would you like your results? Paper is the default. PAPER DISK EMAIL

If submitting more than one search, please prioritize in order of need.

The EIC searcher normally will contact you before beginning a prior art search. If you would like to sit with a searcher for an interactive search, please notify one of the searchers.

Where have you searched so far on this case?

Circle: USPT DWPI EPO Abs JPO Abs IBM TDB

Other: _____

What relevant art have you found so far? Please attach pertinent citations or Information Disclosure Statements. _____

What types of references would you like? Please checkmark:

Primary Refs ☒ Nonpatent Literature _____ Other _____
 Secondary Refs ☒ Foreign Patents _____
 Teaching Refs _____

What is the topic, such as the **novelty**, motivation, utility, or other specific facets defining the desired **focus** of this search? Please include the concepts, synonyms, keywords, acronyms, registry numbers, definitions, structures, strategies, and anything else that helps to describe the topic. Please attach a copy of the abstract and pertinent claims.

Claims 1, 4-7 & 10-12

Problem: See paragraphs 1-5
Solution: " " 6-13

16/9/1 (Item 1 from file: 2)

DIALOG(R) File 2:INSPEC

(c) 2004 Institution of Electrical Engineers. All rts. reserv.

5659967 INSPEC Abstract Number: B9709-7230-078

Title: A strontium titanate thermocapacitive **floating gate** MOS flow sensor

Author(s): Kwang Ming Lin; Chee Yee Kwok; Ruey Shing Huang

Journal: Sensors and Materials vol.9, no.3 p.131-9

Publication Date: 1997 Country of Publication: Japan

CODEN: SENMER ISSN: 0914-4935

Abstract: A new thermocapacitive integrated flow sensor that uses a **floating gate** MOS transistor has been fabricated. Perovskite strontium titanate (SrTiO_3) is used as a dielectric material between the top (**control**) **gate** and the **floating gate**. The temperature dependence of the **dielectric constant** is about 2000 ppm/ degrees C. The process flow is compatible with standard MOS processes and augmented to include a new capacitor module and bulk micromachining at the final step. The output drain voltage change at a flow velocity of 26 m/s is about 57 mV. Sensitivity in the linear range is 5.5 mV (m/s)/sup -1/. (17 Refs)

Copyright 1997, IEE

16/9/2 (Item 2 from file: 2)
DIALOG(R) File 2:INSPEC
(c) 2004 Institution of Electrical Engineers. All rts. reserv.

5271169 INSPEC Abstract Number: B9607-7230-003

Title: An integrated thermo-capacitive type MOS flow sensor

Author(s): Kwang Ming Lin; CheeYee Kwok; Ruey Shing Huang

Journal: IEEE Electron Device Letters vol.17, no.5 p.247-9

Publisher: IEEE,

Publication Date: May 1996 Country of Publication: USA

CODEN: EDLEDZ ISSN: 0741-3106

Abstract: A prototype of a new thermo-capacitive integrated flow sensor consisting of a **floating-gate** MOS transistor has been developed. Tantalum pentoxide is the dielectric material between the top (**control**) **gate** and the **floating-gate**. The temperature dependence of the **dielectric constant** is about 375 ppm/ degrees C. The process flow is compatible with standard MOS process and augmented to include a capacitor module and bulk micromachining. The output voltage change at the flow velocity of 20 m/s is about 26 mV at 57 mW of heater power. The sensitivity in the 0-4 m/s flow velocity region is 4.25 mV(m/s)/sup -1/. (7 Refs)

Class Codes: B7230 (Sensing devices and transducers); B7320W (Level, flow and volume measurement); B2575 (Micromechanical device technology); B2560R (Insulated gate field effect transistors)

Chemical Indexing:

Ta2O5 int - Ta2 int - O5 int - Ta int - O int - Ta2O5 bin - Ta2 bin - O5 bin - Ta bin - O bin (Elements - 2)

Copyright 1996, IEE

16/9/3 (Item 3 from file: 2)
 DIALOG(R) File 2:INSPEC
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04047326 INSPEC Abstract Number: B9201-1285-010, C9201-5330-002

Title: **Floating gate** structures as nonvolatile analog memory cells in 1.0 μ m-LOCOS-CMOS technology with PZT dielectrics

Author(s): Soennecken, A.; Hilleringmann, U.; Goser, K.

Journal: Microelectronic Engineering vol.15, no.1-4 p.633-6

Publication Date: Oct. 1991 Country of Publication: Netherlands

CODEN: MIENEF ISSN: 0167-9317

Abstract: In this paper a new **floating gate** structure of a nonvolatile analog memory cell in 1.0 μ m-LOCOS-CMOS technology is proposed. The new **floating gate** transistor with $\text{Pb}(\text{Zr};\text{Ti})\text{O}/\text{sub } 3/$ as dielectrics between the **control** and **floating gate** needs no additional coupling area. After the description of the device fabrication basic characteristics of the ferroelectric material PZT and the new transistor cell are presented. In comparison to measurements on standard **floating gate** structures it is pointed out that the use of PZT increases or preserves the programming efficiency in spite of a considerable reduction in cell area. In the face of high leakage currents through PZT the memory cells without an additional coupling area can be programmed. For a sufficient support of the tunnel mechanism and for an utilization of the high **dielectric constant** of $\text{Pb}(\text{Zr};\text{Ti})\text{O}/\text{sub } 3/$ a dielectric combination of $\text{SiO}/\text{sub } 2/$ and PZT in analog memory cells seems to be efficient to avoid the occurred leakage current. (5 Refs)

Chemical Indexing:

$\text{PbZrO}_3\text{TiO}_3$ ss - TiO_3 ss - ZrO_3 ss - O_3 ss - Pb ss - Ti ss - Zr ss - O ss
 (Elements - 4)

$\text{SiO}_2\text{-PbZrO}_3\text{TiO}_3$ int - $\text{PbZrO}_3\text{TiO}_3$ int - SiO_2 int - TiO_3 int - ZrO_3 int - O_2 int - O_3 int - Pb int - Si int - Ti int - Zr int - O int - $\text{PbZrO}_3\text{TiO}_3$ ss - TiO_3 ss - ZrO_3 ss - O_3 ss - Pb ss - Ti ss - Zr ss - O ss - SiO_2 bin - O_2 bin - Si bin - O bin (Elements - 2,4,5)

Numerical Indexing: size 1.0E-06 m

2/17/04

09/990,397

16/9/4 (Item 1 from file: 8)
DIALOG(R) File 8: Ei Compendex(R)
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04405794 E.I. No: EIP96053192010

Title: Integrated thermo-capacitive type MOS flow sensor

Author: Lin, Kwang Ming; Kwok, CheeYee; Huang, Ruey Shing

Source: IEEE Electron Device Letters v 17 n 5 May 1996. p 247-249

Publication Year: 1996

CODEN: EDLEDZ ISSN: 0741-3106

Abstract: A prototype of a new thermo-capacitive integrated flow sensor consisting of a **floating-gate** MOS transistor has been developed. Tantalum pentoxide is the dielectric material between the top(**control**) **gate** and the **floating-gate**. The temperature dependence of the **dielectric constant** is about 375 ppm/ degree C. The process flow is compatible with standard MOS process and augmented to include a capacitor module and bulk micromachining. The output voltage change at the flow velocity of 20 m/s is about 26 mV at 57 mW of heater power. The sensitivity in the 0-4 m/s flow velocity region is 4.25 mV(m/s)** minus **1. (Author abstract) 7 Refs.

Descriptors: Sensors; MOSFET devices; Flow measurement; Gates (transistor); Dielectric materials; **Permittivity**; Capacitors; Micromachining; Temperature; Tantalum compounds

16/9/5 (Item 1 from file: 34)
DIALOG(R) File 34:SciSearch(R) Cited Ref Sci
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05985771 Genuine Article#: XM174 Number of References: 17
Title: A strontium titanate thermocapacitive **floating gate** MOS
flow sensor

Author(s): Lin KM; Kwok C; Huang RS

Journal: SENSORS AND MATERIALS, 1997, V9, N3, P131-139

ISSN: 0914-4935 Publication date: 19970000

Publisher: MYU K K, SCIENTIFIC PUBLISHING DIV, 2-32-3 SENDAGI, BUNKYO-KU,
TOKYO 113, JAPAN

Abstract: A new thermocapacitive integrated flow sensor that uses a
floating gate MOS transistor has been fabricated.
Perovskite strontium titanate (SrTiO_3) is used as a dielectric material
between the top (**control**) **gate** and the **floating**
gate. The temperature dependence of the **dielectric**
constant is about 2000 ppm/degrees C. The process flow is
compatible with standard MOS processes and augmented to include a new
capacitor module and bulk micromachining at the final step. The output
drain voltage change at a flow velocity of 26 m/s is about 57 mV.
Sensitivity in the linear range is 5.5 mV (m/s) (-1).

20/9/2 (Item 2 from file: 2)
 DIALOG(R) File 2:INSPEC
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6616753 INSPEC Abstract Number: A2000-14-7330-001, B2000-07-2530D-009

Title: Band offsets of wide-band-gap oxides and implications for future electronic devices

Author(s): Robertson, J.

Journal: Journal of Vacuum Science & Technology B (Microelectronics and Nanometer Structures) Conference Title: J. Vac. Sci. Technol. B, Microelectron. Nanometer Struct. (USA) vol.18, no.3 p.1785-91

Publisher: AIP for American Vacuum Soc,

Publication Date: May-June 2000 Country of Publication: USA

CODEN: JVTBD9 ISSN: 0734-211X

Abstract: Wide-band-gap oxides such as SrTiO_3 are shown to be critical tests of theories of Schottky barrier heights based on metal-induced gap states and charge neutrality levels. This theory is reviewed and used to calculate the Schottky barrier heights and band offsets for many important high **dielectric constant** oxides on

Pt and Si. Good agreement with experiment is found for barrier heights. The band offsets for electrons on Si are found to be small for many key oxides such as SrTiO_3 and Ta_2O_5 which limit their utility as gate oxides in future silicon field effect transistors. The calculations are extended to screen other proposed oxides such as BaZrO_3 , ZrO_2 , HfO_2 , La_2O_3 , Y_2O_3 , HfSiO_4 , and ZrSiO_4 . Predictions are also given for barrier heights of the ferroelectric oxides $\text{Pb}_{1-x}\text{Zr}_x\text{TiO}_3$ and $\text{SrBi}_2\text{Ta}_2\text{O}_9$ which are used in **nonvolatile memories**. (83 Refs)

Subfile: A B

Descriptors: barium compounds; bismuth compounds; dangling bonds; **energy gap**; hafnium compounds; insulated gate field effect transistors; interface states; lanthanum compounds; lead compounds; Schottky barriers; strontium compounds; tantalum compounds; yttrium compounds; zirconium compounds

Identifiers: wide-band-gap oxides; band offsets; device implications; Schottky barrier heights; metal-induced gap states; charge neutrality levels; high **dielectric constant** oxides; gate oxides; ferroelectric oxides; **nonvolatile memories**; interface gap states; dangling bond states; band lineups; SrTiO_3 ; Ta_2O_5 ; BaZrO_3 ; ZrO_2 ; HfO_2 ; La_2O_3 ; Y_2O_3 ; HfSiO_4 ; ZrSiO_4 ; $\text{SrBi}_2\text{Ta}_2\text{O}_9$; PZT; $\text{PbZrO}_3\text{TiO}_3$

Class Codes: A7330 (Surface double layers, Schottky barriers, and work functions); A7320 (Electronic surface states); B2530D (Semiconductor-metal interfaces); B2560R (Insulated gate field effect transistors)

L64 ANSWER 6 OF 15 HCAPLUS COPYRIGHT 2004 ACS on STN
AN 2000:623720 HCAPLUS
TI Method of fabricating a semiconductor device with a composite gate
dielectric layer and gate barrier **layer**
IN Gardner, Mark I.; Gilmer, Mark C.
PA Advanced Micro Devices, Inc., USA
PI US 6114228 A 20000905 US 1998-120245 19980721
US 6163060 A 20001219 US 1998-163673 19980930 <--
PRAI US 1998-120245 A3 19980721 <--
AB The present invention is directed to a new semiconductor device and a
method for making same. The new semiconductor device is comprised of a
gate barrier **layer**, a composite gate **dielec. layer**, a conductor
layer, and at least one source/drain region formed in a semiconducting
substrate. The method comprises forming the gate barrier **layer**,
composite gate **dielec. layer** and conductor **layer**, patterning those
layers, and forming at least one source/drain region in said
semiconductor substrate. The composite gate **dielec. layer** is
comprised of at least two different materials having different **dielec.**
consts.
IC ICM H01L021-3205
ICS H01L021-00
NCL 438585000

(Has SiO₂ only)
BaTiO₃

L64 ANSWER 8 OF 15 \ HCAPLUS COPYRIGHT 2004 ACS on STN
 AN 2000:238023 HCAPLUS
 TI Flash memory device having **high permittivity stacked dielectric**
 and fabrication thereof
 IN Gardner, Mark I.; Gilmer, Mark C.; Spikes, Thomas E., Jr.
 PA Advanced Micro Devices, USA
 PI US 6048766 A 20000411 US 1998-172410 19981014 <--
 PRAI US 1998-172410 19981014 <--
 AB A memory device having a high performance **stacked dielec. sandwiched**
 between two polysilicon plates and method of fabrication thereof is
 provided. A memory device, in accordance with an embodiment, includes two
 polysilicon plates and a **high permittivity dielec. stack** disposed
 between the two polysilicon plates. The **high permittivity dielec.**
stack includes a relatively **high permittivity layer** and two
 relatively **low permittivity buffer layers**. Each buffer layer is
 disposed between the relatively **high permittivity layer** and a resp.
 one of the two polysilicon plates. The **high permittivity layer** may,
 for example, be a barium strontium titanate and the buffer layers may each
 include a layer of silicon nitride adjacent the resp. polysilicon plate
 and a layer of titanium dioxide between the silicon nitride and the barium
 strontium titanate. The new high performance **dielec. layer** can, e.g.,
 increase the speed and reliability of the memory device as compared to
 conventional memory devices.
 IC ICM H01L021-336
 NCL 438257000
 IT 7440-21-3, Silicon, uses **7631-86-9**, Silica, uses 12033-89-5,
 Silicon nitride, uses **13463-67-7**, Titania, uses 37305-87-6,
 Barium strontium titanate
 RL: DEV (Device component use); USES (Uses)
 (flash memory device having **high permittivity**
stacked dielec. and fabrication thereof)
 IT **7631-86-9**, Silica, uses **13463-67-7**, Titania, uses
 RL: DEV (Device component use); USES (Uses)
 (flash memory device having **high permittivity**
stacked dielec. and fabrication thereof)
 RN 7631-86-9 HCAPLUS
 CN Silica (6CI, 7CI, 8CI, 9CI) (CA INDEX NAME)
 RN 13463-67-7 HCAPLUS
 CN Titanium oxide (TiO2) (8CI, 9CI) (CA INDEX NAME)

L64 ANSWER 8 OF 15 HCAPLUS COPYRIGHT 2004 ACS on STN
 AN 2000:238023 HCAPLUS
 TI Flash memory device having **high permittivity stacked dielectric**
 and fabrication thereof
 IN Gardner, Mark I.; Gilmer, Mark C.; Spikes, Thomas E., Jr.
 PA Advanced Micro Devices, USA
 PI US 6048766 A 20000411 US 1998-172410 19981014 <--
 PRAI US 1998-172410 19981014 <--
 AB A memory device having a high performance **stacked dielec. sandwiched**
 between two polysilicon plates and method of fabrication thereof is
 provided. A memory device, in accordance with an embodiment, includes two
 polysilicon plates and a **high permittivity dielec. stack** disposed
 between the two polysilicon plates. The **high permittivity dielec.**
stack includes a relatively **high permittivity layer** and two
 relatively **low permittivity buffer layers**. Each buffer layer is
 disposed between the relatively **high permittivity layer** and a resp.
 one of the two polysilicon plates. The **high permittivity layer** may,
 for example, be a barium strontium titanate and the buffer layers may each
 include a layer of silicon nitride adjacent the resp. polysilicon plate
 and a layer of titanium dioxide between the silicon nitride and the barium
 strontium titanate. The new high performance **dielec. layer** can, e.g.,
 increase the speed and reliability of the memory device as compared to
 conventional memory devices.
 IC ICM H01L021-336
 NCL 438257000
 IT 7440-21-3, Silicon, uses **7631-86-9**, Silica, uses 12033-89-5,
 Silicon nitride, uses **13463-67-7**, Titania, uses 37305-87-6,
 Barium strontium titanate
 RL: DEV (Device component use); USES (Uses)
 (flash memory device having **high permittivity**
stacked dielec. and fabrication thereof)
 IT **7631-86-9**, Silica, uses **13463-67-7**, Titania, uses
 RL: DEV (Device component use); USES (Uses)
 (flash memory device having **high permittivity**
stacked dielec. and fabrication thereof)

L64 ANSWER 10 OF 15 HCAPLUS COPYRIGHT 2004 ACS on STN
 AN 1999:405201 HCAPLUS
 TI Fabrication of high **dielectric constant** insulator for gate contact for semiconductor devices
 IN Gardner, Mark I.; Fulford, H. Jim
 PA Advanced Micro Devices, Inc., USA
 PI US 6258675 B1 20010710 US 1997-993766 19971218
 PRAI US 1997-993766 A 19971218 <--
 AB A gate insulator having a high **dielec. const.** is disclosed. In one embodiment of the invention, the method includes three steps. In the 1st step, a gate insulator layer is formed on a substrate. The gate insulator layer includes at least one **layer**, having a high **dielec. const.** In the 2nd step, a gate conductor is formed on the gate insulator layer, the gate conductor masking a portion of the gate insulator layer. In the 3rd step, the gate insulator layer is removed, except for the portion masked by the gate conductor. In a particular embodiment, the gate insulator is formed by depositing Si₃N₄, then Ta₂O₅ or TiO₂, then Si₃N₄. Then depositing and patterning gate polysilicon. Then oxidizing polysilicon. Then etching the two uppermost gate insulator layers. Then implanting and annealing source and drain. Then remove the oxide which was formed on the polysilicon. Results in upper gate insulator layers being wider than gate polysilicon.
 IC ICM H01L021-28
 ICS H01L021-336; H01L029-51
 IT **1314-61-0**, Tantalum oxide (Ta₂O₅) **7440-21-3**, Silicon, processes **7631-86-9**, Silica, processes **12033-89-5**, Silicon nitride (Si₃N₄), processes **13463-67-7**, Titanium oxide (TiO₂), processes
 RL: DEV (Device component use); PEP (Physical, engineering or chemical process); PROC (Process); USES (Uses)
 (fabrication of high **dielec. const.** insulator for gate contact for semiconductor devices)
 IT **1314-61-0**, Tantalum oxide (Ta₂O₅) **7631-86-9**, Silica, processes **13463-67-7**, Titanium oxide (TiO₂), processes
 RL: DEV (Device component use); PEP (Physical, engineering or chemical process); PROC (Process); USES (Uses)
 (fabrication of high **dielec. const.** insulator for gate contact for semiconductor devices)

L64 ANSWER 11 OF 15 HCAPLUS COPYRIGHT 2004 ACS on STN
AN 1999:818236 HCAPLUS
TI Floating gate avalanche injection MOS transistors with **high K**
dielectric control gates
IN Gregor, Richard William; Kizilyalli, Isik C.; Roy, Pradip Kumar
PA Lucent Technologies Inc., USA
PI US 6008091 > A 19991228 US 1998-14030 19980127
PRAI US 1998-14030 A 19980127 <--
AB The invention relates to a process for making a MOS Si device, i.e., a
MOSFET DRAM LSI, esp. intergate dielecs. between the floating silicon gate
and the control silicon gate in MOS memory devices. The intergate
dielecs. are composite structures of SiO₂-Ta₂O₅-SiO₂ with the first SiO₂
layer grown on the floating gate,, and all layers preferably produced in
situ in an LPCVD reactor. After formation of the composite SiO₂ --Ta₂O₅
--SiO₂ dielec., it is annealed at low pressure to densify the SiO₂ layers.
Elec. measurements show that the charge trap d. in the intergate **dielec.**
is substantially lower than in **layered dielecs.** produced by prior
techniques.
IC ICM H01L029-788
NCL 438261000
IT **1314-61-0**, Tantalum pentoxide 7440-21-3, Silicon, processes
7631-86-9, Silica, processes
RL: DEV (Device component use); PEP (Physical, engineering or chemical
process); PROC (Process); USES (Uses)
(floating gate avalanche injection MOS transistor with **high**
K dielec. control gate)

L64 ANSWER 14 OF 15 HCAPLUS COPYRIGHT 2004 ACS on STN
 AN 1985:141881 HCAPLUS
 TI Thin-film integrated device
 IN Nomura, Koji; Ogawa, Hisahito; Abe, Atsushi; Nitta, Tsuneharu
 PA Matsushita Electric Industrial Co., Ltd. , Japan
 PI WO 8403992 A1 19841011 WO 1984-JP145 19840329 <--
 JP 05063947 B4 19930913 JP 1983-57552 19830331
 JP 04006277 B4 19920205 JP 1983-98343 19830602
 EP 139764 A1 19850508 EP 1984-901397 19840329 <--
 EP 139764 B1 19891018
 PRAI JP 1983-57552 19830331 <--
 JP 1983-98343 19830602 <--
 AB In a thin-film integrated device having ≥ 1 thin-film element(s) on
 an insulator substrate, the thin-film element(s) consists of an insulator
 thin film of a sputter-deposited complex oxide contg. Ta and Al. The
 insulator film has a high dielec. const., high dielec.-breakdown
 field strength, and low leakage current. Optionally, the integrated
 device may be comprised of a ZnS electroluminescent display device and
 thin-film element(s) may consist of a thin-film capacitor, CdSe FET,
 and/or LED.
 IC H01B003-12; H01G004-10; H05B033-22; H01L049-02; H01L029-78; H01C017-12;
 C23C015-00
 IT 1314-61-0D, solid solns. with alumina 1344-28-1D, solid
 solns. with tantalum oxide
 RL: DEV (Device component use); TEM (Technical or engineered material
 use); USES (Uses)
 (elec. insulators, for thin-film integrated devices)
 IT 1314-61-0D, solid solns. with alumina 1344-28-1D, solid
 solns. with tantalum oxide
 RL: DEV (Device component use); TEM (Technical or engineered material
 use); USES (Uses)
 (elec. insulators, for thin-film integrated devices)
 RN 1314-61-0 HCAPLUS
 CN Tantalum oxide (Ta2O5) (8CI, 9CI) (CA INDEX NAME)
 RN 1344-28-1 HCAPLUS
 CN Aluminum oxide (Al2O3) (8CI, 9CI) (CA INDEX NAME)

L64 ANSWER 15 OF 15 HCAPLUS COPYRIGHT 2004 ACS on STN
AN 1984:415942 HCAPLUS
TI Permanent memory
IN Sato, Nobuyuki; Uchiumi, Kyotake; Nabetani, Shinji; Uchida, Ken
PA Hitachi, Ltd., Japan; Hitachi Microcomputer Engineering Ltd.
PI DE 3334557 A1 19840405 DE 1983-3334557 19830923 <--
PRAI JP 1982-164910 19820924 <--
AB A ROM cell with a high integration d. and low operating potential is
prepd. by depositing a Si film of 1 cond. type on a Si substrate of
another type, forming a SiO2 isolation film, depositing a Si3N4 **film**
with a different **dielec. const.**, forming gate contacts, forming an
intermediate insulator layer, doping, and forming more gates.
IC G11C017-04; H01L021-314; H01L027-00
IT **7631-86-9**, uses and miscellaneous
RL: USES (Uses)
(in ROM fabrication)
RN 7631-86-9 HCAPLUS
CN Silica (6CI, 7CI, 8CI, 9CI) (CA INDEX NAME)